CLAIMS

1. Process for making a semiconductor device comprising the following steps:

- a doped region (44.1) with a first type of conductivity is made on a first principal face (40.2) of a semiconductor substrate (40), and at least one window (45) is made delimiting said region,

- a first metallisation area (46) is deposited on the doped region (44.1) with the first type of conductivity,

- a dielectric layer (47) is deposited on at least the window (45) and the first metallisation area (46),

- at least a first opening (48) is etched in the dielectric layer (47) at the window (45) exposing the substrate (40) that will accommodate a doped region (50) with a second type of conductivity while arranging an undoped portion (40.1) of the semiconductor substrate laterally between the doped region (50) with the second type of conductivity and the doped region (44.1) with the first type of conductivity,

- the substrate (40) is doped to create the doped region (50) with the second type of conductivity,

- a second metallisation area (50) is deposited covering the dielectric layer (47) and coming into contact with the doped region (50) with the second type of conductivity.

2. Process according to claim 1, characterised in that the doped region (44.1) with the first type of conductivity is made by deposition of a doped layer (44) with the first type of conductivity on the principal face (40.2) of the substrate and etching the window exposing the substrate in the doped layer with this first type of conductivity.

3. Process according to claim 1, characterised in that the doped region (44.1) with the first type of conductivity is made by the formation of a dielectric layer (55) on the principal face (40.2) of the substrate, by stripping a part of the dielectric (55) using a stripping paste by screen printing forming a stripped area around the contour of the future doped region with the first type of conductivity, then doping the stripped area, and then removing the remaining dielectric (55) to form the window.

4. Process according to claim 1, characterised in that the doped region (44.1) with the first type of conductivity is made by the formation of a dielectric layer (55) on the principal face (40.2) of the substrate, by stripping a part of the dielectric (55) using a stripping paste by screen printing forming a stripped area around the contour of the future doped region with the first type of conductivity and then doping the stripped area, the remaining dielectric (55) forming the window (55.1).

5. Process according to claim 1, characterised in that at least one etching is a laser etching.

6. Process according to claim 1, characterised in that at least one of the etchings is a screen printing etching.

7. Process according to claim 1, characterised in that at least one metallisation area is made by screen printing.

8. Process according to claim 1, characterised in that the doped region (44.1) with the first type of conductivity and the doped region (50) with the second type of conductivity are nested in each other.

9. Process according to claim 1, characterised in that the first opening (48) is smaller in area than the window (45).

10. Process according to claim 1, characterised in that the first metallisation area (46) is deposited on the doped region (44.1) with the first type of conductivity before or after the window (45) etching step.

11. Process according to claim 2, characterised in that etching of the doped layer (44) with the first type of conductivity attacks the semiconductor substrate (40).

12. Process according to claim 1, characterised in that deposition step for the second metallisation area (51) precedes the doping step of the substrate (40) in which the doped region (50) with the second type of conductivity is created, the material in the second metallisation area (51) being annealed so as to diffuse into the substrate at the first opening (48).

13. Process according to claim 1, characterised in that the substrate (40) comprises a stack with a weakened layer (41) and a thin layer (43), the weakened layer being in depth, the principal face (40.2) of the substrate on which the doped

layer (44) with the first type of conductivity is deposited being a face of the thin layer.

14. Process according to claim 13, characterised in that it comprises a step to fix the second metallisation area (51) onto an electrically insulating support (52).

15. Process according to claim 14, characterised in that it comprises a step to dissociate the thin layer (43) from the substrate at the weakened layer (41).

16. Process according to claim 15, characterised in that it comprises a step for protection and passivation of the thin layer (43) on the side on which it was dissociated.

17. Process according to claim 1, characterised in that the step to etch the first opening (48) includes etching of a second opening (49) at the first metallisation area (46) exposing a metallisation strip (46.1) within the first metallisation area (46).

18. Process according to claim 17, characterised in that the deposition step for the second metallisation area (51) does not cover the second opening (49).

19. Process according to claim 1, characterised in that the device is formed from one or several solar cells (35).

20. Process according to claim 19, characterised in that the solar cells are connected in series and / or in parallel.